ABSTRACT OF THE DISCLOSURE

A vertical structure high carrier mobility transistor on a substrate of crystalline silicon doped with impurities of the N type, the transistor having a collector region located at a lower portion of the substrate. The transistor includes a heterostructure alloy region positioned in the substrate and comprised of a heterostructure alloy of silicon and germanium. A base region is positioned in the substrate above the first conducting region and doped with P-type impurities. A first dielectric layer is positioned on, and directly contacts, the heterostructure alloy region, and defines a first window directly above the heterostructure alloy region. The transistor also includes an emitter positioned in the heterostructure alloy region and between the first window and the base region. The emitter is comprised of the heterostructure alloy doped with impurities of the first type and directly contacts the first dielectric layer.